Question Paper Code : 71393

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2015.

Sixth Semester

Computer Science and Engineering

CS 2354/CS 64/10144 CS 604 — ADVANCED COMPUTER ARCHITECTURE

(Regulation 2008/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Briefly describe data hazards.
2. Point out the different types of data dependences.
3. Differentiate between VLIW and EPIC Processors.
4. Briefly describe about the Register Stack Mechanism in IA-64 Register model.
5. What is the use of branch prediction buffer?
6. Write a note on multiprocessor cache coherence.
7. Point out how RAID can improve the performance of I/O.
8. What is the need to implement memory as a hierarchy?
9. Enlist the features of SMT Architecture.
10. Point out the advantages and disadvantages of heterogeneous multi-core processors.

PART B — (5 × 16 = 80 marks)

11. (a) Explain how compiler technology can be used to enhance a processor's ability to exploit ILP.

Or

(b) What are the different ways for branch prediction? Discuss how pipeline performance issues can be reduced by branch prediction.

12. (a) Discuss about Itanium processor and its IA 64 Instruction Set architecture.

Or

(b) What is speculative execution? Compare and contrast hardware and software speculation mechanisms.

13. (a) Discuss in detail about the performance issues in symmetric and distributed shared memory architectures.

Or

(b) What is the need of memory consistency model? Explain its various types.

14. (a) Describe the need of cache optimization scheme. Give a description about the advanced cache optimization schemes to reduce cache miss penalty and miss rate.

Or

(b) Elaborate on the different methods to measure the performance of I/O.

15. (a) Compare and contrast Intel Multi core architecture and SUN CMP Architecture.

Or

(b) What is hardware multithreading? Compare and contrast Fine grained Multi-Threading and Coarse grained Multi–Threading.

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