B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2014.

Third Semester

Computer Science and Engineering

CS 2202/CS 34/EC 1206 A/080230012/10144 CS 303 — DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2008/2010)

(Common to PTCS 2202 – Digital Principles and System Design for B.E. (Part-Time) Second Semester – CSE – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert 231.3_{10} to binary.

2. Simplify $z = (AB + C)(B'D + C'E') + (AB + C)'$.

3. Realize $G = AB'C + DE + F'$ using NAND gates.

4. Realise 4-bit binary to gray code converter using EX-OR gates.

5. State the difference between demultiplexer and decoder.

6. State the difference between PAL and PLA.

7. Write the HDL code to realize a D flip flop.

8. State the rules for state assignment.

9. What are cycles and races?

10. Draw the ASM chart for the following state diagram.

PART B — (5 × 16 = 80 marks)
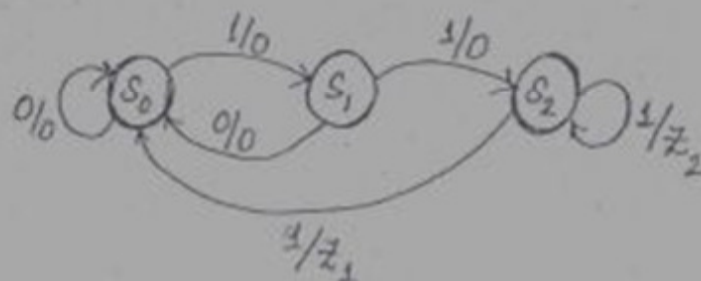
11. (a) (i) Add, subtract and multiply the following numbers in binary 110010 and 11101. (6)

    (ii) Minimize the following function using Karnaugh map. (10)
    $f(A, B, C, D) = \sum m (0, 1, 2, 3, 4, 5, 6, 11, 12, 13)$.

Or

    (b) (i) State and prove De Morgan's theorems for 2 variables. (6)

    (ii) Simplify the following function using Quine - Mc Cluskey method (10)
    $f(a, b, c, d) = \sum m (0, 1, 2, 5, 6, 7, 8, 9, 10, 14)$.

12. (a) (i) Design a 2-bit binary magnitude comparator. (6)

    (ii) Design a 2-bit binary multiplier to multiply two binary numbers and produce a 4-bit result. (10)

Or

    (b) (i) Design a full adder and realize it using only NOR gates. (8)

    (ii) Design a 4- bit parallel binary adder/subtractor. (8)

13. (a) (i) Implement the following function using 8 to 1 multiplexer (10)
    $f(a, b, c, d) = \sum m (0, 1, 3, 5, 9, 12, 14, 15)$.

    (ii) Write the HDL code to realize binary to octal encoder. (6)

Or

    (b) (i) Design 8 to 3 priority encoder. (8)

    (ii) Simplify the following functions and implement it using a suitable PLA. $F(A, B, C, D) = \sum m (0, 2, 4, 6, 8, 10, 12, 14)$ and $G = \prod M (1, 3, 5, 7)$.

14. (a) Design a sequence detector to detect the input sequence 101 (overlapping). Use JK flip flops. (16)

Or

    (b) (i) Design a 3-bit synchronous up counter using JK flip flops. (6)

    (ii) Design a 3-bit parallel in serial out shift register and write the HDL code to realize it. (10)

15. (a) (i) Explain the two types of asynchronous sequential circuits with suitable examples. (10)

    (ii) What is a flow table? Explain with a suitable example. (6)

Or

    (b) (i) What are the basic building blocks of an ASM chart? Explain. (6)

    (ii) What is an hazard? How to remove hazards using hazard covers in Karnaugh map? Explain. (10)

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