B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2013.

Third Semester

Computer Science and Engineering

CS 2202/CS 34/EC 1206 A/10144 CS 303/080230012 — DIGITAL PRINCIPLES AND SYSTEMS DESIGN

(Common to Information Technology)

(Regulation 2008/2010)

(Common to PTCS 2202 – Digital Principles and Systems Design for B.E. (Part-Time) Second Semester – CSE – Regulation 2009)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(101101.1101)_2$ to decimal and hexadecimal form.

2. What are the limitations of Karnaugh map?

3. Write down the truth table of a full subtractor.

4. What is meant by Test Bench?

5. Distinguish between a decoder and a demultiplexer.

6. Compare SRAM and DRAM.

7. Derive the characteristic equation of a JK-flipflop.

8. What is a Mealy circuit?

9. What is primitive flow table?

10. What are static '1' and static '0' hazards?

PART B — ($5 \times 16 = 80$ marks)

11. (a) Reduce the following functions using Karnaugh map technique :

(i) $f(A, B, C) = \Sigma m\,(0, 1, 3, 7) + \Sigma d(2, 5)$

(ii) $F(w, x, y, z) = \Sigma m(0, 7, 8, 9, 10, 12) + \Sigma d(2, 5, 13)$.

Or

(b) Simplify the Boolean function using Quine McCluskey method :

$F(A, B, C, D, E, F) = \Sigma m(0, 5, 7, 8, 9, 12, 13, 23, 24, 25, 28, 29, 37, 40, 42, 44, 46, 55, 56, 57, 60, 61)$.

12. (a) Design a full adder using 2 half adders.

Or

(b) Design a combinational circuit to convert binary to gray code.

13. (a) Implement the switching function $F = \Sigma m\,(0, 1, 3, 4, 12, 14, 15)$ using an 8 input MUX.

Or

(b) Implement the switching functions

$Z_1 = a\bar{b}\,\bar{d}\,e + \bar{a}\,\bar{b}\,\bar{c}\,\bar{d}\,\bar{e} + bc + de$

$Z_2 = \bar{a}\,\bar{c}\,e$

$Z_3 = bc + de + \bar{c}\,\bar{d}\,\bar{e} + bd$

$Z_4 = \bar{a}\,\bar{c}\,e + ce$ using $5 \times 8 \times 4$ PLA.

14. (a) Using D flip-flops, design a synchronous counter which counts in the sequence, 000, 001, 010, 011, 100, 101, 110, 111, 000.

Or

(b) Design a shift register using JK flipflops.

15. (a) (i) Explain the types of hazards in digital circuits.

(ii) Implement the switching function $F = \Sigma m(1, 3, 5, 7, 8, 9, 14, 15)$ by a static hazard free 2 level AND-OR gate network.

Or

(b) Explain the steps for the design of asynchronous sequential circuits.